

1 / 13

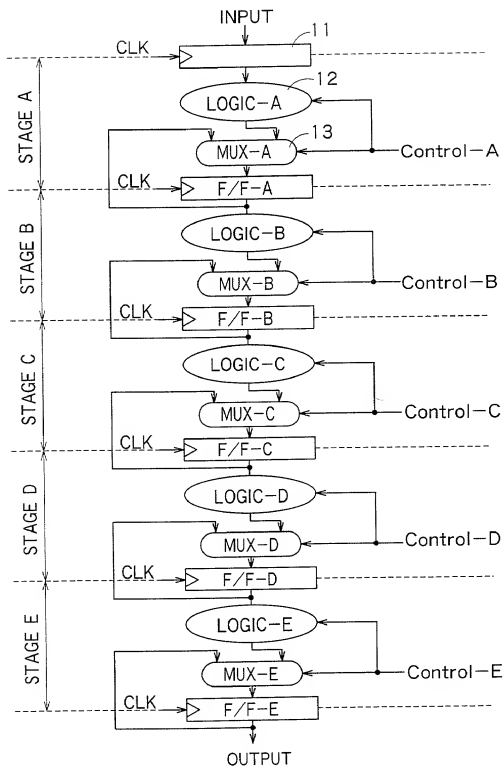


FIG. 1

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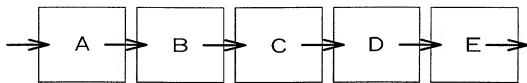


FIG. 2

RF: Register File  
 IR : Instruction Register  
 IC : Instruction Cache

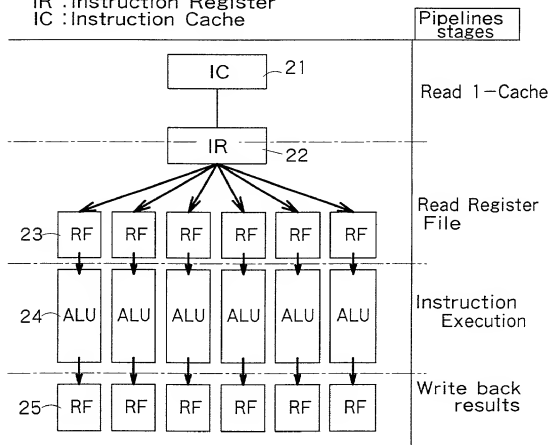


FIG. 3

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Control all pipeline flipflops

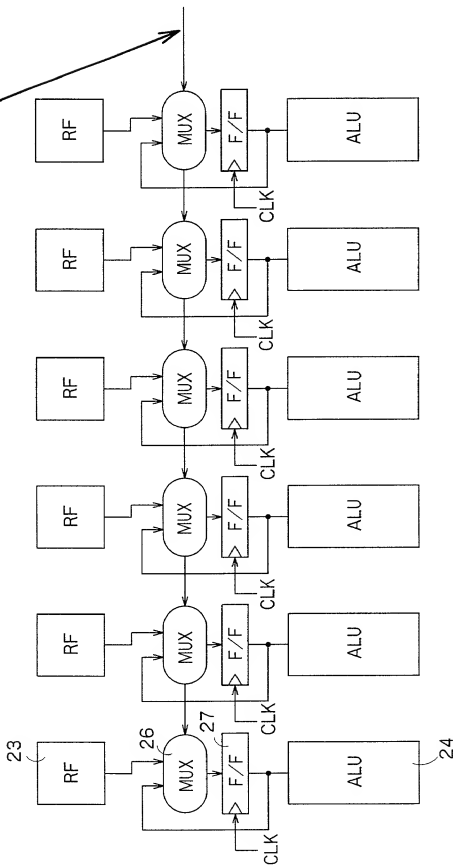


FIG. 4

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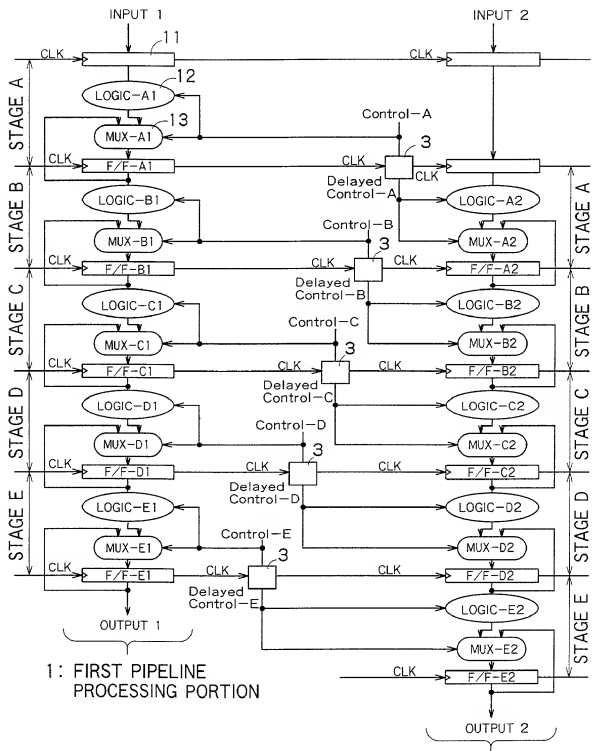


FIG. 5

2: SECOND PIPELINE  
PROCESSING PORTION

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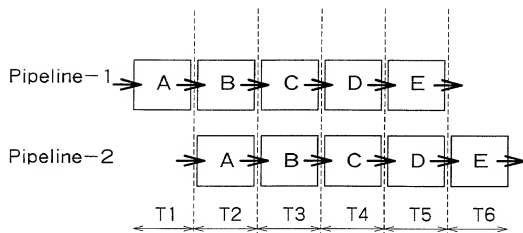


FIG. 6A

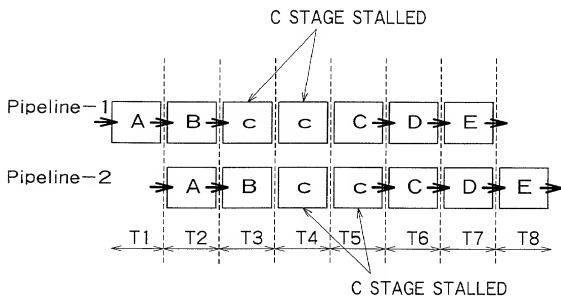


FIG. 6B

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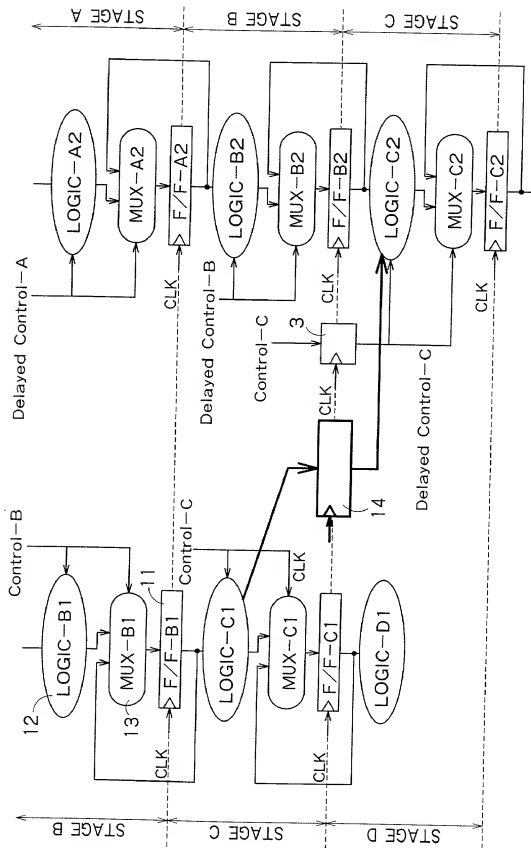


FIG. 7

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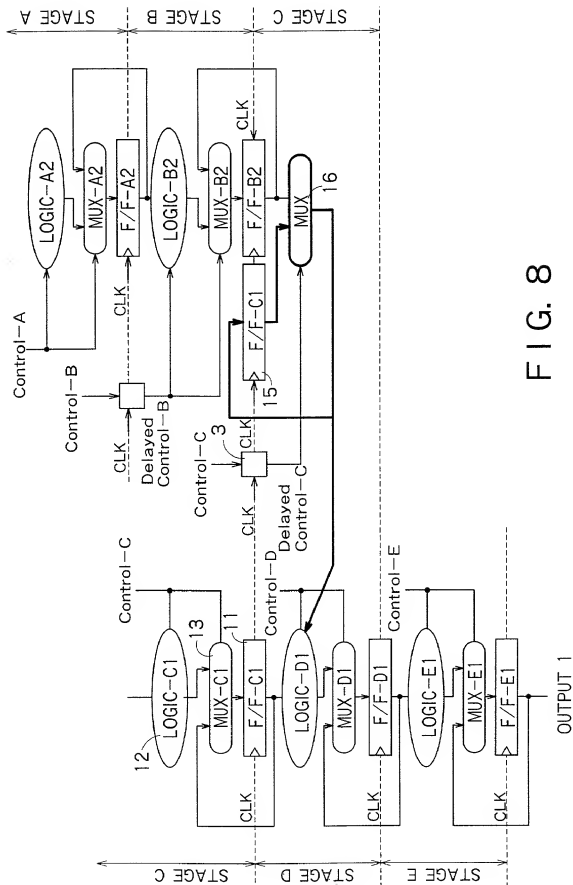


FIG. 8

FIG. 8

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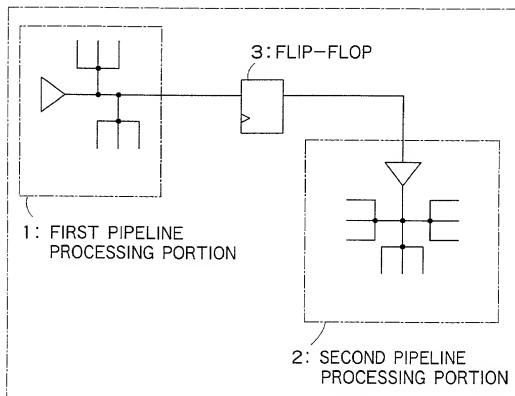


FIG. 9



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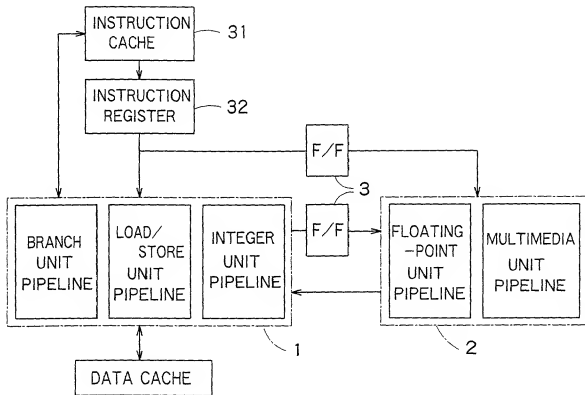


FIG. 10

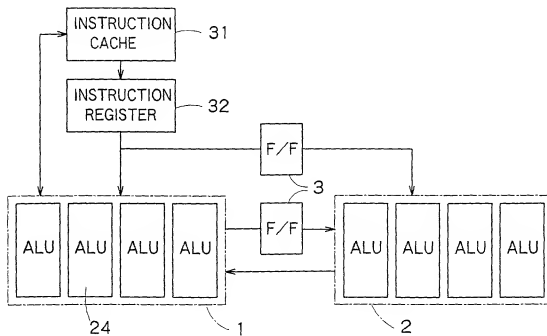


FIG. 11

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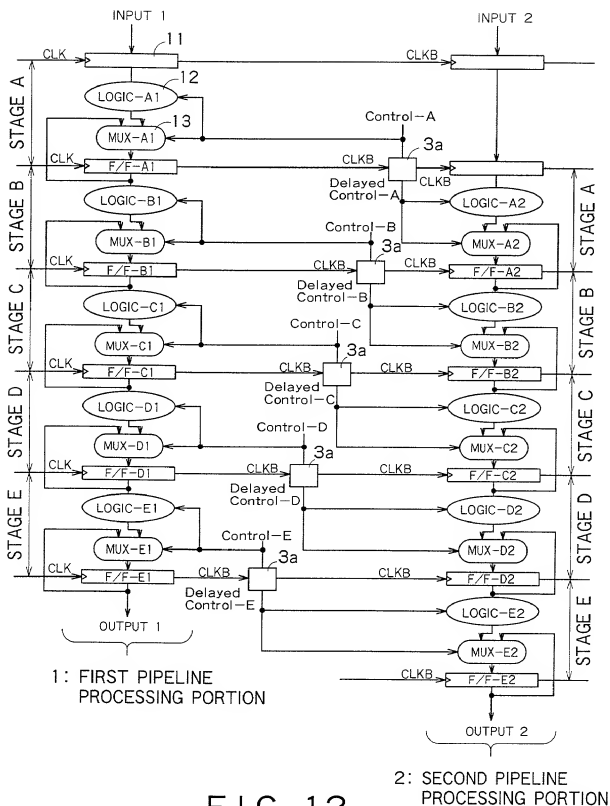


FIG. 12

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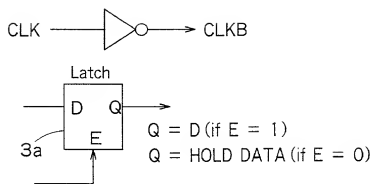


FIG. 13

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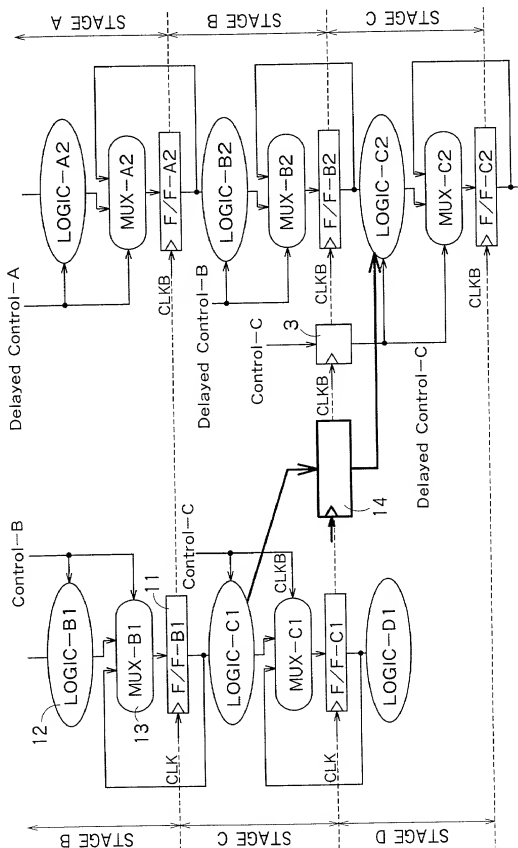


FIG. 14

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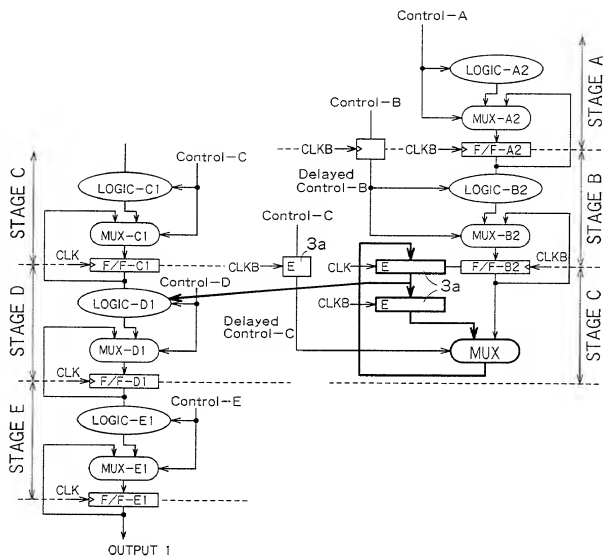


FIG. 15